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10/045,564	01/09/2002	Stacey G. Lloyd	BEA920000019US1	1831

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EXAMINER	
BUEHL, BRETT J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,564	LLOYD, STACEY G.	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 7-19 have been examined. Applicant has canceled claims 6 and 20.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 3/5/05.

Withdrawn Rejections

3. Applicant, via amendment, has overcome the 35 U.S.C. 102 and 103 rejections set forth in the previous Office Action. Consequently, the examiner has withdrawn these rejections.

Claim Objections

4. Claim 11 is objected to because of the following informalities: the last limitation of the claim contains the phrase "programmed list of responses", which should be "preprogrammed list of responses" as it was in the original claims (i.e. a change was made with no indication that it is supposed to be changed). Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or d escribed in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-9 and 11-19 are rejected under 35 U.S.C. 102(b) as being anticipated by the IBM Technical Disclosure Bulletin, Vol. 37 No. 03, hereinafter IBM.

7. Regarding claim 1, IBM has taught a method for handling operations within a hardware device, comprising:

a. Providing within the device information regarding an operation ***[Instruction Register of Figure 2. The instruction register contains, and therefore provides, information regarding an operation (i.e. an instruction).]***, the operation having a predetermined responsive output as encoded within a transaction lookup table ***[Programmable Decode Array of Figure 2. The programmable decode array contains predetermined responsive outputs for instructions.]***, the provided information including information identifying the operation ***[It is inherent that the provided information contains an opcode field, the opcode identifying the operation.]***.

b. Selecting at least some of the identifying information of the operation to output to a comparator and the transaction lookup table [***Instruction Register output of Figure 2. The output of the instruction register is an opcode. The opcode is input into the comparator (i.e. a portion of the Combinational Logic for Hardwired Decoder) and the transaction lookup table (i.e. Programmable Decode Array). A portion of the hardwired decoder logic is functionally a comparator as it takes the opcode as an input and outputs a response dependent on the input. In other words, it compares the opcode to the hardwired instructions and outputs a corresponding response.***], and output of the

comparator and output of the transaction lookup table are input into a multiplexer ***[Figure 2. The circled portion of Figure 2 is an N-bit 2-to-1 multiplexer. The extrinsic evidence in Kime et al. shows the logic of a Quadruple 2-to-1 Line Multiplexer (N=4) to be identical to that of the circled logic (the enable bit is an optional feature in Kime, which is absent). The comparator and programmable decode array both output to the multiplexer.]***;

c. Selecting an alternative responsive output for the operation instead of the predetermined responsive output based upon the selected identifying information resulting in the comparator directing the multiplexer to output the alternative responsive output ***[Reserved Invalid of Figure 2. The reserved invalid bit, which is output from the comparator, selects an alternative response as output by the comparator when the comparator determines that the opcode is not reserved/invalid. The reserved invalid bit is input to the multiplexer as the selection bit, which enables one of the two inputs to become the output. When it is logic "0", the output from the comparator is the output.]***, such that the multiplexer effectively converts at least some of the information regarding the operation based upon the selected identifying information ***[The multiplexer converts the at least some of the information by outputting the decoded instruction, the decoded instruction output being dependent on the identifying information.]***;

d. Executing the operation based upon the converted information ***[It is inherent that the operation is executed based on the converted information.]***.

8. Regarding claim 2, IBM has taught the method of claim 1, wherein the provided information is within a register of the device ***[Instruction Register of Figure 2. The provided information (i.e. the instruction) is within the instruction register of the device.]***.

9. Regarding claim 3, IBM has taught the method of claim 1, wherein the identifying information is within a register of the device ***[Instruction Register of Figure 2. The identifying information is part of the provided information, which is within the instruction register. Therefore, it is also within the instruction register.]***.

10. Regarding claim 4, IBM has taught the method of claim 1, wherein the converted information is within a register of the device ***[Register (output of Programmable Decode Array) of Figure 2. The output of the programmable decode array is the converted information as output by the multiplexer and is contained in the register.]***.

11. Regarding claim 5, IBM has taught the method of claim 1, wherein the step of providing information regarding the operation comprises providing the predetermined responsive output and the alternative output ***[Figure 2. The predetermined responsive output (i.e. output from the programmable decode array) and the alternative responsive output (i.e. output from the combination logic for hardwired decoder) are both provided to the multiplexer.]***.

15. Regarding claim 8, IBM has taught a method for redirecting transactions within a hardware device, wherein transactions occurring within said device contain fields of information regarding the transaction, the method comprising the steps of:

a. Loading all of said fields necessary to identify a transaction into a first register ***[Instruction Register of Figure 2. The instruction register contains all of the necessary information to identify a transaction.]***;

b. Selecting which fields of said register are to be acted upon and inputting the selected fields into a multiplexer ***[It is inherent that the designer selected which fields were to be acted upon and those fields are input into the multiplexer.];***

c. Converting the transaction information to be redirected through a pre-programmed value for each said field by inputting into the multiplexer a predetermined responsive value into the multiplexer, the multiplexer also receiving input from a comparator, such that the multiplexer outputs an alternative responsive value for the transaction ***[N-bit 2-to-1 Mux of Figure 2 (circled logic). The multiplexer selects a substitute response, that of the programmable decode array, in place of the "normal" response output by a portion of the combinational decode logic when the comparator indicates the "reserved invalid" signal.]***; and

d. Outputting said new transaction results to a register ***[Register (output of Programmable Decode Array) of Figure 2. The output of the programmable decode array is the new transaction results as output by the multiplexer and is contained in the register. Therefore, the new transaction results are output into a register.]***.

16. Regarding claim 9, IBM has taught the method of claim 8, wherein the step of loading said field necessary to identify a transaction includes first loading transaction identifications ***[It is inherent that the transaction identifications are loaded into the instruction register.]***.

17. Regarding claim 11, IBM has taught a method for redirecting operations within a hardware device, wherein operations occurring within said device contain fields of information regarding the operation and such operations are compared with a preprogrammed list of

responses and the hardware device issues responses based on each operation, the method comprising the steps of:

a. Creating a list of identified operations for which a redirected response is desired ***[It is inherent that a designer of IBM created a list of instructions for which a redirected response is desired.]***;

b. Comparing an operation with the list of said identified operations using a comparator ***[Combinational Logic for Hardwired Decoder of Figure 2. A portion of the hardwired decoder logic is functionally a comparator as it takes the opcode as an input and outputs a response dependent on the input (e.g. Reserved Invalid signal). In other words, it compares the opcode to the hardwired instructions and outputs a corresponding response.]***;

c. Outputting results of the comparator and a preprogrammed response from the preprogrammed list of responses for the operation into a multiplexer, such that output of the multiplexer represents the redirected response for the operation ***[N-bit 2-to-1 Mux of Figure 2 (circled logic). The multiplexer selects a substitute response, that of the programmable decode array, in place of the "normal" response output by a portion of the combinational decode logic when the comparator indicates the "reserved invalid" signal.]***; and

d. Substituting the redirected response for the preprogrammed response from said preprogrammed list of responses ***[It is inherent that the substitute response replaces the standard response given the functionality of the multiplexer (i.e. only one of them is outputted.]***.

12. Regarding claim 12, IBM has taught the method of claim 11, wherein the step of creating a list of identified operations includes first loading transaction identifications ***[It is inherent that when the designer creates the list of identified operations he/she "loads" the transaction identifications by hardwiring them in the logic.]***.

13. Regarding claim 14, IBM has taught a system for altering predetermined response comprised of:

a. First storage means to identify operations for which a response different from said predetermined response is desired ***[Instruction Register of Figure 2. The register is a storage means used to identify operations for which a response different from said predetermined response is desired by outputting the opcode of the operation to the combinational decode logic and the map logic.]***;

b. Comparator means to compare said given operation with said identified operations ***[Combinational Logic for Hardwired Decoder of Figure 2. A portion of the hardwired decoder logic is functionally a comparator as it takes the opcode as an input and outputs a response dependent on the input (e.g. Reserved Invalid signal). In other words, it compares the opcode to the hardwired instructions and outputs a corresponding response.]***;

c. Second storage means to load a substitute response for said predetermined response, the second storage means comprising a plurality of registers ***[Programmable Decode Array of Figure 2. The programmable decode array contains "substitute" responses for identified operations. The programmable decode array comprises a plurality of registers, as the term "register" is defined***

as a device capable of temporarily storing a value. Since the programmable decode array is "programmable", it temporarily stores values.]; and

d. Selection means to select said substitute response when a given operation meets a predefined criteria for substituting a response from said second storage means, the selection means comprising a multiplexer into which the predetermined response is input and output from the plurality of registers is input, such that output of the comparator means is employed to select the output of the plurality of registers in lieu of the predetermined response as the substitute response ***[N-bit 2-to-1 Mux of Figure 2 (circled logic). The multiplexer selects a substitute response, that of the programmable decode array, in place of the "normal" response output by a portion of the combinational decode logic when the comparator indicates the "reserved invalid" signal.]***.

13. Regarding claim 15, IBM has taught the system of claim 14, wherein one or more of said storage means may be selectively enabled or disabled ***[Instruction Register of Figure 2. It is inherent that the instruction register has a "write enable" signal input into the register. This is means that the register may be selectively enabled or disabled for receiving an instruction. Therefore, it may be selectively enabled or disabled.]***.

14. Regarding claim 16, IBM has taught in a data system utilizing a hardware control device in which a given operation results in a predetermined response for that operation, a system for providing a programmable redefinition of allowed instructions and associated responses within said hardware device including:

a. First register means which contains fields to identify preselected operations which may occur within the system ***[Instruction Register of Figure 2. The instruction register contains fields that are used to identify preselected operations, which may occur within the system by outputting the opcode of the operation to the map logic and the combinational decode logic.]***;

b. Second register means which operates upon selected fields in the first register means to further define a criteria for which redirecting a response is desired ***[Programmable Decode Array of Figure 2. The programmable decode array operates on the opcode of the operation which further defines the criteria for which redirecting a response is desired. The programmable decode array comprises a register means, as the term "register" is defined as a device capable of temporarily storing a value. Since the programmable decode array is "programmable", it temporarily stores values until it is reprogrammed.]***;

c. Comparator means which compares the identified operations with a current operation ***[Combinational Logic for Hardwired Decoder of Figure 2. A portion of the hardwired decoder logic is functionally a comparator as it takes the opcode as an input and outputs a response dependent on the input (e.g. Reserved Invalid signal). In other words, it compares the opcode to the hardwired instructions and outputs a corresponding response.]***;

d. Transaction lookup table means to output a standard value for the current operation ***[Combinational Logic for Hardwired Decoder of Figure 2. The combinational decoder is a "transaction lookup table" in the form of***

combinational logic. When a transaction is to be looked-up, the opcode of the transaction is applied to the inputs and the corresponding response is output. Since each operation has a distinct output, the function of the combinational decoder is a table lookup.]; and

e. Multiplexer means receiving input from the comparator means and the transaction lookup table means and outputting a substitute value for the current operation ***[N-bit 2-to-1 Mux of Figure 2 (circled logic). The multiplexer selects a substitute response, that of the programmable decode array, in place of the "normal" response output by a portion of the combinational decode logic when the comparator indicates the "reserved invalid" signal.]***.

15. Regarding claim 17, IBM has taught the system of claim 16, wherein one or more of said register means may be selectively enabled or disabled ***[Instruction Register of Figure 2. It is inherent that the instruction register has a "write enable" signal input into the register. This is means that the register may be selectively enabled or disabled for receiving an instruction. Therefore, it may be selectively enabled or disabled.]***.

16. Regarding claim 18, IBM has taught a data processing system for executing an operation, comprising:

a. An identification store including information identifying at least selected operations ***[Map and Programmable Decode Array of Figure 2. The map logic inherently contains the opcodes of at least the identified instructions, as it maps each opcode to a corresponding entry of the programmable decode array.]***;

b. A comparator responsive to the operation and the identifying information ***[Combinational Logic for Hardwired Decoder of Figure 2. A portion of the hardwired decoder logic is functionally a comparator as it takes the opcode as an input and outputs a response dependent on the input (e.g. Reserved Invalid signal). In other words, it compares the opcode to the hardwired instructions and outputs a corresponding response. It is responsive to the operation's identifying information, the opcode.]***; and

c. A substitute value responsive to the comparator and the operation ***[Programmable Decode Array of Figure 2. The "substitute value" is contained in an entry of the programmable decode array.]***.

d. A standard value responsive to the comparator and the operation ***[Combinational Logic for Hardwired Decoder of Figure 2. The "standard" response is output by a portion of the combinational logic.]***; and

e. A multiplexer into which the substitute value, the standard value, and output from the comparator are input, and that outputs one of the substitute value and the standard value based on the output from the comparator ***[N-bit 2-to-1 Mux of Figure 2 (circled logic). The multiplexer selects a substitute response, that of the programmable decode array, in place of the "normal" response output by a portion of the combinational decode logic when the comparator indicates the "reserved invalid" signal.]***.

16. Regarding claim 19, IBM has taught the system of claim 1, wherein the comparator is responsive to a mask of the identifying information ***[Since only the opcode of the transaction is***

sent to the comparator (i.e. portion of the combinational logic for hardwired decoder), the comparator is responsive to a mask of the transaction, the remainder of the transaction having been masked out.].

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the IBM Technical Disclosure Bulletin, Vol. 37 No. 03, hereinafter IBM, and further in view of "The PowerPC Architecture: A specification for a new family of RISC processors", hereinafter PowerPC.

18. Regarding claim 7, IBM has taught the method of claim 5 wherein the operation identifications comprise a field for operation identification (OPCD field, PowerPC, Page 21) but has not explicitly disclosed the operation identifications comprising length (L field, PowerPC, Page 21), attribute (RA field, PowerPC, Page 22) and target (BF field, PowerPC, Page 19) of each operation.

19. However, the PowerPC Architecture has taught operation identifications in instructions comprising fields for operation identification (OPCD field, PowerPC), length (L field,

PowerPC), attribute (RA field, PowerPC) and target (BF field, PowerPC) of each operation. One of ordinary skill in the art would have recognized that using the PowerPC Architecture as the architecture in the method/apparatus of IBM would be beneficial given the expansive software base that is compatible with the PowerPC architecture. Using an architecture with such wide acceptance in the field allows for the method/apparatus to run a wide variety of programs, making it more robust for users. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the PowerPC architecture in the method/apparatus of IBM in order to provide an established architecture with an expansive collection of compatible software programs.

19. Regarding claim 10, given the similarities between the claims, the arguments as stated for claim 7 are applicable.

Response to Arguments

20. Applicant's arguments with respect to claims 1, 8, 11, 14, 16 and 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl whose telephone number is (571) 272-4161. The examiner can normally be reached on Monday-Friday 9:00 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 262-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJB
Brett Buehl
May 3, 2005

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